

### AMENDMENTS TO THE CLAIMS

Please amend claims 1-4, 6, 8, 9, 12, 16, 21, 22, 39, 40, and 42-46, and add new claims 47-52, as indicated below.

1. (Currently Amended) A semiconductor package comprising:  
~~a substrate;~~

a first semiconductor chip ~~coupled to a surface of the substrate, the first semiconductor chip~~ having opposed first and second surfaces ~~which are substantially flat in nature;~~

an adhesive layer coupled to the second surface of the first semiconductor chip;

a second semiconductor chip stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces ~~which are substantially flat in nature; and~~

an insulator coupled to and covering the entire first surface of the second semiconductor chip, ~~for preventing shorting of wirebonds wherein the insulator is coupled between the adhesive layer and the first surface of the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof.~~

2. (Currently Amended) A semiconductor package in accordance with Claim 1 further comprising:

at least one ~~input-output~~ pad ~~being~~ formed on the second surface of the first semiconductor chip; and

at least one first conductive wire connecting the ~~input-output~~ at least one pad of the first semiconductor chip and ~~the~~ a substrate.

3. (Currently Amended) A semiconductor package in accordance with Claim 2 further comprising:

at least one ~~input-output pads~~ pad formed on the second surface of the second semiconductor chip; and

at least one second conductive wire connecting the ~~input-output pads~~ at least one pad of the second semiconductor chip and the substrate.

4. (Currently Amended) A semiconductor package in accordance with Claim 3 wherein the first semiconductor chip is an edge pad type semiconductor chip in which the ~~input-output~~ at least one pad of the first semiconductor chip is formed at an inner circumference of the second surface.

5. (Original) A semiconductor package in accordance with Claim 3 wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

6. (Currently Amended) A semiconductor package in accordance with Claim 3 wherein the adhesive layer covers a part of the at least one first conductive wire positioned on the ~~input-output~~ at least one pad of the first semiconductor chip.

7. (Original) A semiconductor package in accordance with Claim 3 wherein the insulator is one selected from a group consisting of:

a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

8. (Currently Amended) A semiconductor package in accordance with Claim 3 wherein a first end of the at least one first conductive wire is bonded on the substrate by ball bonding

and a second end of the at least one first conductive wire is bonded on the ~~input-output~~ at least one pad of the first semiconductor chip by stitch bonding.

9. (Currently Amended) A semiconductor package in accordance with Claim 8 wherein a conductive ball is formed on the ~~input-output~~ at least one pad of the first semiconductor chip bonded by the stitch bonding.

10-11. (Cancelled)

12. (Currently Amended) A semiconductor package in accordance with Claim 3 wherein a first end of the at least one first conductive wire is bonded on the substrate and a second end of the at least one first conductive wire is bonded on the ~~input-output~~ at least one pad of the first semiconductor chip by stitch bonding.

13-15. (Cancelled)

16. (Currently Amended) A semiconductor package in accordance with Claim 3 wherein a section of the at least one first conductive wires is contacted with the insulator.

17-20. (Cancelled)

21. (Currently Amended) A semiconductor package comprising:  
~~a substrate;~~  
a first semiconductor chip ~~coupled to a surface of the substrate, the first semiconductor chip~~ having opposed first and second surfaces ~~which are substantially flat in nature, the~~ second surface including a plurality of pads;

an adhesive layer coupled to the second surface of the first semiconductor chip; and

a second semiconductor chip stacked over the second surface of the first semiconductor chip and having opposed first and second surfaces ~~which are substantially flat in nature~~; and

~~means~~ an insulator coupled to the first surface of the second semiconductor chip, ~~for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the means for preventing shorting of wirebonds~~

wherein the insulator is coupled between the first surface of the second semiconductor chip and the adhesive layer, and is between the first surface of the second semiconductor chip and each of the pads of the second surface of the first semiconductor chip.

22. (Currently Amended) A semiconductor package in accordance with Claim 21 further comprising:

at least one ~~input-output~~ pad ~~being~~ formed on the second surface of the first semiconductor chip;

at least one first conductive wire connecting the at least one ~~input-output~~ pad of the first semiconductor chip and ~~the~~ a substrate;

at least one ~~input-output pads~~ pad formed on the second surface of the second semiconductor chip; and

at least one second conductive wire connecting the ~~input-output pads~~ at least one pad of the second semiconductor chip and the substrate.

23-32. (Cancelled)

33-38. (Cancelled)

39. (Currently Amended) A semiconductor package comprising:  
a substrate;  
a first semiconductor chip coupled to ~~a surface of the~~ substrate, the first semiconductor chip having opposed first and second surfaces ~~which are substantially flat in nature~~;  
a second semiconductor chip having opposed first and second surfaces ~~which are substantially flat in nature~~;  
a first means coupled to the second surface of the first semiconductor chip for ~~adhering~~ coupling the first semiconductor chip to the second semiconductor chip in a stack;  
~~means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof;~~  
at least one ~~input-output~~ pad being formed on the second surface of the first semiconductor chip; and  
at least one first conductive wire connecting the at least one ~~input-output~~ pad of the first semiconductor chip and the substrate;  
at least one ~~input-output pads~~ pad formed on the second surface of the second semiconductor chip; ~~and~~  
at least one second conductive wire connecting the at least one pad ~~input-output pads~~ of the second semiconductor chip and the substrate; and  
an insulator coupled between to the first surface of the second semiconductor chip and the first means, and overlying both the first means and the at least one first conductive wire.

40. (Currently Amended) A semiconductor package in accordance with Claim 39 wherein the first means coupled to the second surface of the first semiconductor chip is an adhesive layer.

41. (Previously Added) A semiconductor package in accordance with Claim 40 wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

42. (Currently Amended) A semiconductor package in accordance with Claim 39 wherein the ~~means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds~~ insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

43. (Currently Amended) A semiconductor package in accordance with Claim 39 wherein a first end of the at least one first conductive wire is bonded on the substrate by ball bonding and a second end of the at least one first conductive wire is bonded on the ~~at least input-output~~ at least one pad of the first semiconductor chip by stitch bonding.

44. (Currently Amended) A semiconductor package in accordance with Claim 43 wherein a conductive ball is formed on the at least one ~~input-output~~ pad of the first semiconductor chip bonded by the stitch bonding.

45. (Currently Amended) A semiconductor package in accordance with Claim 39 wherein a first end of the at least one first conductive wire is bonded on the substrate and a second end of the at least one first conductive wire is bonded on the

at least one ~~input-output~~ pad of the first semiconductor chip by stitch bonding.

46. (Currently Amended) A semiconductor package in accordance with Claim 45 wherein a first end of the at least one first conductive wire is bonded on the substrate and a second end of the at least one first conductive wire is bonded on the at least one ~~input-output~~ pad of the first semiconductor chip by stitch bonding.

47. (New) A semiconductor package in accordance with Claim 39, further comprising a sealing material covering the substrate, the first and second semiconductor chips, and the at least one first and second conductive wires, wherein a portion of the sealing material is between the pads of the second surface of the first semiconductor chip and the insulator.

48. (New) A semiconductor package in accordance with Claim 1, further comprising a sealing material covering the first and second semiconductor chips, wherein a portion of the sealing material is between the second surface of the first semiconductor chip and the insulator.

49. (New) A semiconductor package in accordance with Claim 1, further comprising a sealing material covering the first and second semiconductor chips, wherein a portion of the sealing material is between the second surface of the first semiconductor chip and the insulator.

50. (New) A semiconductor package comprising:  
a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;

a plurality of conductive wires, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip;

a second semiconductor chip stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface, and an opposite second surface that includes a plurality of pads;

an insulator coupled to the first surface of the second semiconductor chip, said insulator being between each of the conductive wires and the first surface of the second semiconductor chip;

an adhesive layer coupled between the insulator and the first surface of the second semiconductor chip; and

a sealing material covering the first and second semiconductor chips, wherein a portion of the sealing material is between the pads of the second surface of the first semiconductor chip and the insulator.

51. (New) A semiconductor package comprising:

a first semiconductor chip having opposed first and second surfaces, the second surface including a plurality of pads;

a plurality of conductive wires, wherein each of the conductive wires is electrically coupled to a respective one of the pads of the first semiconductor chip;

a second semiconductor chip stacked over the second surface of the first semiconductor chip, the second semiconductor chip including a first surface, and an opposite second surface that includes a plurality of pads;

an insulator coupled to the first surface of the second semiconductor chip, said insulator being between the pads of the second surface of the first semiconductor chip and the first surface of the second semiconductor chip; and

an adhesive layer coupled between the insulator and the first surface of the second semiconductor chip, the adhesive layer being entirely inward of the pads of the second surface of the first semiconductor chip.

52. (New) A semiconductor package in accordance with Claim 51, further comprising a sealing material covering the first and second semiconductor chips, wherein a portion of the sealing material is between the pads of the second surface of the first semiconductor chip and the insulator.